Listing of Claims

Claims 1-18 (cancelled)

19. (currently amended) A power-on bias circuit comprising:

a first inverter having an input terminal and an output terminal, said input terminal of the first inverter functions as a first voltage input terminal for said power-on bias circuit;

a second inverter having an input terminal and an output terminal, wherein said output terminal of said second inverter functions as an output terminal for said power-on bias circuit; and

a Schmitt Trigger circuit comprising:

a first P-type transistor;

a second P-type transistor, wherein a substrate of said second P-type transistor, a substrate and a source region of said first P-type transistor are electrically connected to a second voltage input terminal of said power-on bias circuit, a source region of the second P-type transistor is electrically connected to a drain region of said first P-type transistor; wherein the second voltage input terminal receives a voltage signal of high potential when peripheral circuits are turned on before turning on core circuits, wherein the first voltage input terminal receives the voltage signal of high potential when the core circuits are turned on;

a first N-type transistor;

a second N-type transistor, a gate of said first P-type transistor, a gate of said second P-type transistor, a gate of said first N-type transistor and a gate of said second N-type transistor are electrically connected to said input terminal for said Schmitt Trigger circuit, said input terminal of the Schmitt Trigger circuit is electrically connected to said output terminal of said first inverter, a substrate of said first N-type transistor, a substrate and a source region of said second N-type transistor are electrically connected to ground, a drain region of said second N-type transistor is electrically connected to a source region of said first N-type transistor;

a third P-type transistor, a source region of said third P-type transistor is electrically connected to said drain region of the first P-type transistor and said source region of the second P-type transistor, a drain region of said third P-type transistor is electrically connected to ground, a substrate of said third P-type transistor is electrically connected to said second voltage input terminal of said power-on bias circuit; and

a third N-type transistor, a source region of said third N-type transistor is electrically connected to a source region of said first N-type transistor and a drain region of said second N-type transistor, a drain region of said third N-type transistor is electrically connected to said second voltage input

terminal of said power-on bias circuit, a substrate of said third N-type transistor is electrically connected to ground, a drain region of said second P-type transistor, a drain region of said first N-type transistor, a gate of said third P-type transistor and a gate of said third N-type transistor are electrically connected to said output terminal of the Schmitt Trigger circuit, said output terminal of the Schmitt Trigger circuit is electrically connected to said input terminal of the second inverter.

20. (previously presented) A power-on bias circuit according to claim 19, wherein said first inverter comprises a fourth P-type transistor and a fourth N-type transistor, a substrate and a source region of said fourth P-type transistor is electrically connected to said second voltage input terminal of the power-on bias circuit, a source region of said fourth N-type transistor is electrically connected to ground, a gate of said fourth P-type transistor and a gate of said fourth N-type transistor are electrically connected to said input terminal of said first inverter, a drain region of said fourth P-type transistor and a drain region of said fourth N-type transistor are electrically connected to said output terminal of said second inverter.

21. (previously presented) A power-on bias circuit according to claim 19, wherein said second inverter comprises a fourth P-type transistor and a fourth N-type transistor, a substrate and a source region of said fourth P-type transistor is electrically connected to said second voltage input terminal of the power-on bias circuit, a source region of said fourth N-type transistor is electrically connected to ground, a gate of said fourth P-type transistor and a gate of said fourth N-type transistor are electrically connected to said input terminal of said second inverter.

22. (previously presented) A power-on bias circuit according to Claim 19, wherein said first voltage input terminal of the power-on-bias circuit is a core voltage input terminal, said second voltage input terminal of the power-on-bias circuit is an input terminal of an input/output terminal.

23. (previously presented) A power-on bias circuit according to Claim 20, wherein dimension of the fourth N-type transistor is larger than dimension of the fourth P-type transistor to reduce a leakage current flowing from the second voltage input terminal to the ground.

24. (cancelled)